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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,657	12/18/2001	Gilbert Wolrich	10559/613001/P12852	2667

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EXAMINER	
PATEL, JAY P	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/024,657	WOLRICH ET AL.	
	Examiner	Art Unit	
	Jay P. Patel	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-19 and 21-28* is/are rejected.

7)☒ Claim(s) *14 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 5/15/2006.

2. Claims 1-28 are pending.

3. Claims 1-5, 9-13, 15-19 and 21-25 are rejected.

4. Claims 6-8, 14, 20 and 26-28 are objected to.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 9-13, 15-19 and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Starr (US Patent 6470415 B1).

7. In regards to claim 1, Starr teaches in figure 1 an enqueue operation 60 (written to head units 33 or 35) and a dequeue operation 62 (read from tail units 37 or 39). The enqueue operation 60 and dequeue operation 62 anticipate a first enqueue request and a second dequeue request respectively. Figure 3 is the network computer apparatus where the management of the queues of figure 1 takes place. Figure 5 is the detailed diagram of the queue manger 220 disclosed in figure 3. Starr reveals that the operation of the queue manager is pipelined (column 5, lines 4-5) and discloses an SRAM controller 214 in figure 3 which services the read and write requests by reading the tail

or writing the head of the accessed queue (see figure 3 and column 5, lines 36-40). The SRAM controller 214 anticipates causing to commence processing of the second request prior to completion of processing the first request.

In regards to claim 2, Starr teaches that QRAM 245 in figure 5, stores pointers regarding each queue (see column 5, lines 12-18). The arbiter 235 selects an operation and modifies the variables of QRAM 245 (see column 5, lines 19-23). The pointers anticipate modifying stored information describing a structure of the queue in response to the requests.

In regards to claim 3, the pointers are stored in a QRAM 245. Therefore, the QRAM anticipates storing the modified information in a cache memory.

In regards to claim 4, The QRAM 245 stores pointer relating to the queue as variables related to the queues (see column 5, lines 12-18). Therefore, the QRAM reads on the first and second requests using linked list data structure.

In regards to claim 5, the enqueue operation 60 and dequeue operation 62 anticipate a first enqueue request and a second dequeue request respectively.

8. In regards to claim 9, figure 2 includes a queue controller 14, which, handles enqueuing and dequeuing of entries. Therefore, the queue controller 14 anticipates a processing engine to make enqueue requests and a scheduler to make dequeue request.

Figure 5 includes a QRAM 245 that stores pointers regarding each queue (see column 5, lines 12-18). Therefore, the QRAM 245 anticipates a cache memory to store data describing a structure of a queue

Figure 5 is an illustration of a queue manager 220. The queue manager 220 anticipates a queue manager including a content addressable memory to store a reference (pointer stored in QRAM 245) to data in the cache memory (QRAM 245) describing the structure of the queue.

Starr also reveals an SRAM controller 214 in figure 3 which services the read and write requests by reading the tail or writing the head of the accessed queue (see figure 3 and column 5, lines 36-40). The SRAM controller 214 anticipates the queue manager configured to process the enqueue requests and the dequeue requests and capable of commencing processing a request to a queue while a previous request with respect to same queue is being processed.

In regards to claim 10, DRAM 203 and SRAM 206 anticipate memory to store data placed on a queue.

In regards to claim 11, Starr teaches that the operation in the queue manager is pipelined (see column 5, lines 4-5). Therefore, the pipelined queue manger operation anticipates a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble, and classify data packets to determine an output queue for each packet and to make requests to the queue manager that specify the output queue.

In regards to claim 12, the SRAM controller 214 in figure 3 is coupled to transmit sequencer 215 and queue manager 220. Therefore, the second plurality of pipelined programming engines to receive data from the queue manager and send data to a transmit buffer is anticipated by the connection between the transmit sequencer, the queue manger and the SRAM controller 214.

In regards to claim 13, the transmit sequencer 215 anticipates a scheduler configured to determine the order of packets to be removed from the queue. Figure 4 contains four registers; a positive setting for a specific bit in the Q-Empty register 86 indicates an empty queue (column 4, lines 43-44). The Q-Empty register anticipates a bit for the queue indicating whether the queue is empty.

9. In regards to claim 15, host 170 in figure 3 anticipates a source of data packets.

Device 160 in figure 3 is connected to a network 164. Therefore it is inherent that there is a destination for the data packets.

In further regards, figure 2 includes a queue controller 14, which, handles enqueuing and dequeuing of entries. Therefore, the queue controller 14 anticipates a processing engine to make enqueue requests and a scheduler to make dequeue request.

Figure 5 includes a QRAM 245 that stores pointers regarding each queue (see column 5, lines 12-18). Therefore, the QRAM 245 anticipates a cache memory to store data describing a structure of a queue

Figure 5 is an illustration of a queue manager 220. The queue manager 220 anticipates a queue manager including a content addressable memory to store a reference (pointer stored in QRAM 245) to data in the cache memory (QRAM 245) describing the structure of the queue.

Starr also reveals an SRAM controller 214 in figure 3 which services the read and write requests by reading the tail or writing the head of the accessed queue (see figure 3 and column 5, lines 36-40). The SRAM controller 214 anticipates the queue manager configured to process the enqueue requests and the dequeue requests and capable of commencing processing a request to a queue while a previous request with respect to same queue is being processed.

In regards to claim 16, DRAM 203 and SRAM 206 anticipate memory to store data placed on a queue.

In regards to claim 17, Starr teaches that the operation in the queue manager is pipelined (see column 5, lines 4-5). Therefore, the pipelined queue manger operation anticipates a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble, and classify data packets to determine an output queue for each packet and to make requests to the queue manager that specify the output queue.

In regards to claim 18, the SRAM controller 214 in figure 3 is coupled to transmit sequencer 215 and queue manager 220. Therefore, the second plurality of pipelined programming engines to receive data from the queue manager and send data to a

transmit buffer is anticipated by the connection between the transmit sequencer, the queue manger and the SRAM controller 214.

In regards to claim 19, the transmit sequencer 215 anticipates a scheduler configured to determine the order of packets to be removed from the queue. Figure 4 contains four registers; a positive setting for a specific bit in the Q-Empty register 86 indicates an empty queue (column 4, lines 43-44). The Q-Empty register anticipates a bit for the queue indicating whether the queue is empty.

10. In regards to claim 21, Starr reveals that the operation of the queue manager is pipelined (column 5, lines 4-5) and in particular, an SRAM controller 214 in figure 3 which services the read and write requests by reading the tail or writing the head of the accessed queue (see figure 3 and column 5, lines 36-40). The SRAM controller 214 and the pipelined process of the queue manager anticipates causing to commence processing of a received enqueue or dequeue request with respect to a queue prior to completion of processing a prior enqueue or dequeue request with respect to the same queue.

In regards to claim 22, Starr teaches that QRAM 245 in figure 5, stores pointers regarding each queue (see column 5, lines 12-18). The arbiter 235 selects an operation and modifies the variables of QRAM 245 (see column 5, lines 19-23). The pointers anticipate modifying stored information describing a structure of the queue in response to the requests.

In regards to claim 23, the pointers are stored in a QRAM 245. Therefore, the QRAM anticipates storing the modified information in a cache memory.

In regards to claim 24, The QRAM 245 stores pointer relating to the queue as variables related to the queues (see column 5, lines 12-18). Therefore, the QRAM reads on the first and second requests using linked list data structure.

In regards to claim 25, the enqueue operation 60 and dequeue operation 62 anticipate a first enqueue request and a second dequeue request respectively and commencing the processing of the second (dequeue operation 62) prior to the completion of the first request (enqueue operation 60).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 6-8 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Starr (US Patent 6470415 B1).

13. In regards to claims 6-8 and 26-28, Starr teaches all the limitations of the parent claims 1 and 21 as stated above. Starr fails to explicitly show the first request being dequeue request and the second request being an enqueue request or the first and second request both being enqueue requests and the first and the second requests being dequeue requests.

However, it would have been obvious to one skilled in the art at the time the invention was made to modify the operations of the SRAMs 22 and 30 and DRAM 25 in figure 1 to enable the queue manager 220 (figure 3) to perform the first and second operations as dequeue/enqueue, enqueue/enqueue and dequeue/dequeue requests. The advantage of doing so would enable the queue manager to dynamically perform memory read/write operations in any given order in order to better manage the flow of data through a network apparatus. For example some data may be enqueued in both the SRAM and the DRAM or may to be dequeued and enqueued from one memory to another or may be dequeued from both memories. The motivation to modify would be to have a queue manager that performs all the necessary memory read/write operations in any order possible for better memory control.

Allowable Subject Matter

Claims 14 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay P. Patel whose telephone number is (571) 272-3086. The examiner can normally be reached on M-F 9:00 am - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPP 7/21/06
Jay P. Patel
Examiner
Art Unit 2616

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